ENHANCED SELECTIVITY FOR EPITAXIAL DEPOSITION

Related Application

[0001] This application claims priority under 35 U.S.C. § 119(e) from U.S. Provisional Patent Application Serial Number 60/442,694, entitled "Enhanced Selectivity for Epitaxial Deposition" and filed January 24, 2003. The entire disclosure of this priority document is hereby incorporated by reference in its entirety.

Field of the Invention

[0002] The present invention relates generally to methods for forming integrated circuits, and particularly to selective epitaxial deposition.

Background of the Invention

[0003] Certain electronic components, such as field effect transistors, include a semi-conductive substrate having two distinct diffusion regions. The diffusion regions are generally referred to as a source and a drain. A gate is positioned adjacent the substrate between the source and the drain. Imparting a voltage to the gate sets up an electric field that enables current flow between the source and the drain through a channel in the portion of the substrate adjacent the gate. The substrate typically comprises a bulk monocrystalline silicon substrate having a relatively light concentration of a conductivity enhancing dopant impurity. In other configurations, the substrate comprises a thin layer of lightly doped semi-conductive material disposed over an underlying insulating layer. Such structures are commonly referred to as semiconductor-on-insulator ("SOI") constructions.

[0004] As integrated circuit ("IC") designs become more dense, the length and size of the channel becomes smaller. In addition, the junction depth, which is the thickness of the source or drain, also becomes smaller. As IC features such as channel length, channel size and junction depth become smaller, certain unwanted side effects can occur. For example, a small channel will increase the lateral electric field within the substrate, which can lead to performance degradation. Additionally, small junction depths can prevent adequate silicon consumption during a self aligned silicide ("SALICIDE") process.

[0005] To address these problems, an elevated source/drain ("ESD") structure has been developed. In an ESD structure, a portion of the source and drain regions are elevated above the substrate. For example, a thin epitaxial layer of monocrystalline silicon can be selectively grown from exposed monocrystalline silicon source and drain substrate areas. As used herein, "selective" growth includes, but is not limited to, growth only in particular regions of an underlying structure. For example, in certain applications, selective growth may occur only over non-oxide regions of a substrate, while non-selective growth would occur over an entire substrate, including oxide regions.

Epitaxial deposition of silicon is well known in the semiconductor device processing art, and involves the precipitation of silicon from a source gas onto a crystal lattice. The deposited silicon forms a structure that replicates and extends the underlying crystal lattice. Conventionally used silicon source gases include silane (SiH_4), silicon tetrachloride ($SiCl_4$), trichlorosilane ($SiHCl_3$) and dichlorosilane (SiH_2Cl_2).

[0006] Additional background information on selective epitaxial deposition of silicon can be found in U.S. Patent 4,578,142 to Corboy, Jr. et al., entitled "METHOD FOR GROWING MONOCRYSTALLINE SILICON THROUGH MASK LAYER" and filed on May 10, 1984. The entire disclosure of this patent is hereby incorporated herein by reference.

[0007] An ESD structure provides sufficient channel length to avoid unwanted side effects, despite the presence of a smaller (narrower) gate. Additionally, sufficient silicon consumption can be provided during the SALICIDE process.

Summary of the Invention

[0008] Thus, it is desired to develop improved methods for forming an elevated source/drain ("ESD") structure. In particular, it is desired to selectively deposit a thin epitaxial layer of monocrystalline silicon on the source and drain regions without causing deposition on any isolation dielectrics (such as oxide regions), as is known in the art.

[0009] Additionally, if a polycrystalline silicon gate is used, undesired polycrystalline silicon will form on the gate during monocrystalline silicon deposition on the source and drain substrate areas. Excessive polycrystalline silicon deposition on the gate can cause the gate to short to the elevated source and drain regions. Excessive polycrystalline

silicon deposition on the gate or elsewhere during the selective deposition can also produce unwanted surface roughness that can present problems in subsequent processing, such as for example, subsequent lithography steps. Therefore, it is desired to minimize or eliminate polycrystalline silicon deposition on the gate during deposition of monocrystalline silicon to form an ESD structure.

[0010] Accordingly, in one embodiment of the present invention, a method of forming an electronic component having elevated active areas includes providing a semiconductor substrate in a processing chamber. The semiconductor substrate has disposed thereon a polycrystalline silicon gate and exposed active areas. The method further includes performing a deposition process in which a silicon-source gas is supplied into the processing chamber to cause polycrystalline silicon to be deposited on the gate and epitaxial silicon to be deposited on the active areas. The method further comprises performing a flash etch back process in which polycrystalline silicon is etched from the gate at a first etching rate and epitaxial silicon is etched from the active areas at a second etching rate. The first etching rate is faster than the second etching rate.

[0011] In another embodiment of the present invention, a method includes providing a semiconductor substrate having a gate and exposed active areas. The method further includes depositing polycrystalline silicon on the gate and epitaxial silicon on the active areas in a first process step. The method further comprises etching polycrystalline silicon from the gate in a second process step. The method further comprises repeating the first and second process steps a plurality of times.

[0012] In another embodiment of the present invention, a method includes providing a semiconductor substrate in a processing chamber. The semiconductor substrate has a first growth region and a second growth region. The method further includes performing a deposition process in which epitaxial growth occurs at an epitaxial growth rate in the first growth region and polycrystalline growth occurs at a polycrystalline growth rate in the second growth region. The method further includes controlling the epitaxial growth rate and the polycrystalline growth rate by periodically pausing the deposition process to perform a flash etch back process. After the flash etch back process, there is more epitaxial growth than polycrystalline growth present on the semiconductor substrate.

[0013] In another embodiment of the present invention, a method includes providing a semiconductor substrate in a processing chamber. The semiconductor substrate has at least one oxide region and at least one non-oxide region. The method further includes alternating a selective epitaxial growth process with a flash etch back process. During the selective epitaxial growth process, epitaxial growth comprising polycrystalline growth and monocrystalline growth occurs in the at least one non-oxide region. Also during the selective epitaxial growth process, substantially no deposition occurs in the at least one oxide region. During the flash etch back process, at least a portion of the polycrystalline growth is etched from the at least one non-oxide region.

Brief Description of the Drawings

[0014] These and other embodiments of the present invention will be readily apparent to the skilled artisan from the following description and the attached drawings.

[0015] FIGURE 1 is a cross-sectional schematic illustration of a conventional field effect transistor, in accordance with the prior art.

[0016] FIGURE 2 is a cross-sectional schematic illustration of the field effect transistor of FIGURE 1 after a selective epitaxial deposition process, in accordance with the prior art.

[0017] FIGURE 3 is a cross-sectional schematic illustration of the field effect transistor of FIGURE 1 after a selective epitaxial deposition process incorporating flash etch back, in accordance with a preferred embodiment of the present invention.

[0018] FIGURE 4 is a flowchart illustrating a cyclical deposition/etching process in accordance with a preferred embodiment of the present invention.

Detailed Description of Preferred Embodiments

[0019] As expounded in detail below, the present disclosure provides methods of fabricating an improved ESD structure. In particular, the present disclosure provides methods for reducing unwanted polycrystalline silicon deposition on a gate region during formation of an elevated ESD structure. However, one of ordinary skill in the art will recognize that the methods disclosed herein also can be applied to any deposition process wherein epitaxial deposition is desired in a first region, while controlled non-epitaxial

deposition at a different rate is desired in a second region. "Controlled" deposition, as used herein, means that the rate of deposition in the second region can vary from 0% to nearly 100% of the rate of epitaxial deposition in the first region.

[0020] FIGURE 1 illustrates the basic structure of a conventional field effect transistor 100. The field effect transistor 100 comprises a substrate 102 and shallow trench isolation regions 104. The substrate 102 is formed of any of the commonly used substrate materials, including silicon, gallium arsenide, or the like. The shallow trench isolation regions 104 can be formed in a conventional manner within the device, and are typically formed of silicon dioxide (SiO_2). The isolation regions 104 can also be formed on the surface of the substrate 102 by partial oxidation of the substrate surface.

[0021] Active areas can be formed within the substrate 102 by various processes, such as by introducing an impurity into the substrate 102 up to several microns deep by ion implantation and activation by rapid thermal annealing ("RTA"). For example, in one embodiment, RTA occurs at approximately 850°C. Preferably, two separate active areas are formed: the source 106 and the drain 108. Both *n*-channel and *p*-channel transistors can be formed in accordance with the various embodiments described herein.

[0022] Still referring to FIGURE 1, a gate dielectric film 114 is formed over the substrate 102. The gate dielectric film 114 typically comprises a layer of SiO_2 that is between 5 nm and 20 nm thick, and is typically grown by thermally oxidizing the underlying silicon substrate 102. However, newer high *k* materials are under investigation. A gate electrode 110 is then formed on the gate dielectric film 114. The gate electrode 110 is typically about 300 nm high, and comprises a conductive material such as polycrystalline silicon, silicon germanium (SiGe) or a metal (such as, for example, tungsten, titanium nitride, and so forth). Conventionally, the gate electrode 110 is formed of polycrystalline silicon (also referred to as "polysilicon"). Insulating sidewall spacers 116 are disposed on the sides of the gate 110. For example, in one embodiment, sidewall spacers 116 comprise a silicon nitride film having a thickness of approximately 20 nm.

[0023] Conventionally used silicon source gases include SiH_4, $SiCl_4$, $SiHCl_3$ and SiH_2Cl_2. As disclosed in U.S. Patent Application 10/074,563, entitled "PROCESS FOR DEPOSITION OF SEMICONDUCTOR FILMS" and filed on February 11, 2002, the entire

disclosure of which is hereby incorporated herein by reference, trisilane (Si_3H_8) can also be used as a silicon source gas. The structure of the field effect transistor 100 after a conventional selective epitaxial growth process is illustrated in FIGURE 2. As illustrated, epitaxial growth occurs over the source 106 and drain 108 depletion regions, thereby forming a monocrystalline silicon elevated source 126 and elevated drain 128 structure. Due to the nature of epitaxial growth, the monocrystalline silicon comprising the elevated source 126 and elevated drain 128 will substantially comprise two dimensional facets.

[0024] In addition, during conventional selective epitaxial deposition, polycrystalline growth occurs on the gate 110, forming a polycrystalline mushroom structure 120 atop the gate. An example of a polycrystalline mushroom structure is illustrated in FIGURE 2. Due to the nature of polycrystalline growth, polycrystalline silicon deposited on the gate 110 during a conventional selective epitaxial deposition stage will substantially comprise multiple three dimensional facets having randomly oriented grains and grain boundaries. This crystalline structure causes the resulting polycrystalline growth to have a mushroom-shaped structure. Such a growth pattern creates the risk of an electrical short between the mushroom structure 120 and the elevated source 126 or elevated drain 128, and therefore can be excessive.

[0025] The presence of a silicon etching gas, such as hydrochloric acid (HCl), during the deposition stage preferably reduces the amount of polycrystalline growth on the isolation regions 104. Specifically, using known selective epitaxy processing techniques, the concentration of HCl present during the deposition stage can be optimized such that no growth is present on isolation regions 104. Additionally, HCl will reduce polycrystalline growth over the gate 110 during the deposition stage, thus increasing the effectiveness of subsequent etching stages.

[0026] To form an ESD structure, the field effect transistor 100 illustrated in FIGURE 1 is subjected to a two stage, deposition/etching cycle. In the first stage, hereinafter referred to as the deposition stage, silicon is deposited from a gas mixture which includes a silicon source gas, a carrier gas, and optionally, an etching precursor.

[0027] The second stage of the silicon deposition/etching cycle is hereinafter referred to as the flash etch back process. In the flash etch back process, a portion of the

material deposited during the deposition stage is etched in a mixture of an etching gas and a carrier gas. For example, in a preferred embodiment wherein silicon deposition was performed in the deposition stage, a conventionally used etching gas is HCl. In such preferred embodiments, other parameters of the flash etch back process are as follows:

TABLE 1

Parameter	Preferred Value	Preferred Range
Temperature	800°C	400 – 1200°C
HCl flow rate	150 sccm	75 – 225 sccm
Carrier gas (H_2) flow rate	60 slm	30 – 90 slm
Pressure	atmospheric	1.0 torr – atmospheric
Etch rate	40 Å min^{-1}	30 – 50 Å min^{-1}
Duration	50% of total deposition period	30% – 70% of total deposition period

In certain embodiments, it may be desirable to conduct the flash etch back process at a higher temperature than the deposition process. One of ordinary skill in the art will recognize that other parameters may be more appropriate for certain applications. In a preferred embodiment, no deposition occurs during the flash etch back process.

[0028] Because polycrystalline silicon over the gate electrode 110 (as well as any polycrystalline silicon deposited on the isolation regions 104 for non-selective embodiments) has a discontinuous grainy three-dimensional structure with multiple facets, the etching gas can attack this structure from all three dimensions. In contrast, the epitaxial growth present over the elevated source 126 and elevated drain 128 has a smooth and flat two-dimensional crystalline structure, and thus etching in those regions will tend to be more two-dimensional. That is, there is more crystal surface exposed to etchants in polycrystalline structures than in monocrystalline structures. This morphological difference between polycrystalline growth and monocrystalline growth causes polycrystalline structures to be etched faster than monocrystalline structures during the flash etch back process. Thus, the net effect of the two stage deposition/etching cycle is to cause epitaxial structures to grow faster than polycrystalline structures over the course of multiple cycles.

[0029] In a preferred embodiment, this two stage deposition/etching cycle is repeated any number of times, until the elevated source/drain structure acquires acceptable dimensions. The relative durations of deposition and etching stages in each cycle are selected to control polycrystalline growth over non-single crystal surfaces relative to epitaxial growth in the active areas. For example, FIGURE 3 illustrates the structure of a field effect transistor 100 after the deposition/etching cycle has been repeated several times, such that the polycrystalline mushroom structure is not present; instead, a polycrystalline cap 130 having acceptable dimensions is present on the gate 110. In particular, because the polycrystalline cap 130 does not have a mushroom structure, there is no conductive material laterally extending directly above the active areas, thus effectively eliminating the risk of creating an electrical short between the polycrystalline cap 130 and the elevated source 126 or elevated drain 130. In other embodiments, polycrystalline growth on the gate 110 can be prevented completely.

[0030] This cyclical deposition/etching process is diagrammatically illustrated in the flowchart of FIGURE 4. As illustrated, selective epitaxial growth in non-dielectric regions is performed in a deposition process 150. Such growth may lead to the existence of unwanted excessive polycrystalline growth in certain regions. To reduce or eliminate such growth, the deposition process is halted in an operational block 155. A flash etch back process 160 is then performed, in which unwanted polycrystalline growth is removed from the dielectric region. If, after the flash etch back process is halted in an operational block 165, additional monocrystalline growth is desired in certain regions (operational block 170), then the process is repeated as necessary.

[0031] Using the two stage deposition/etching cycle described above, selective epitaxial growth to form an ESD structure can be achieved. Separating deposition and etching into multiple successive steps permits the optimization of the deposition and etching steps independently. In particular, stopping deposition and switching to a pure etching process, the ratio of polycrystalline deposition to epitaxial deposition can be minimized, thus allowing a desired thickness of epitaxial growth to be deposited on the source 106 and drain 108, while minimizing the thickness of the polycrystalline cap 130 on the gate 110. Stated more generally, enhanced control of deposition selectivity can be achieved by using the two

stage deposition/etching cycle disclosed herein by selecting an appropriate frequency and duration of the deposition and etching processes.

[0032] In contrast to the two stage deposition/etching cycle disclosed herein, conventional selective epitaxial deposition processes involve adjusting process parameters during deposition such that a high etch rate is maintained on the dielectrics while epitaxial deposition occurs. Such conventional processes are often optimized to eliminate net growth over dielectric regions. In processes that simultaneously etch polycrystalline structures while performing epitaxial growth, a limited ratio of about 20% more epitaxial growth than polycrystalline growth has been achieved. Additionally, such conventional processes suffer from reduced overall process deposition rates due to the presence of simultaneous deposition and etching, especially at low temperatures (for example, below 750 °C).

[0033] The preferred embodiments disclosed above have been described in the context of creating an ESD structure over a polycrystalline gate by modifying selective epitaxial growth. However, the embodiments disclosed herein are for exemplary purposes only, and are not intended to limit the scope of the present invention. For example, one of ordinary skill in the art will recognize that the techniques described herein are readily applicable in other contexts wherein it is desired to control the relative rates of epitaxial and polycrystalline growth in different regions of a substrate. In addition, a wide variety of single or multilevel structures can be made using the two stage deposition/etching cycle disclosed herein.

[0034] The foregoing describes various preferred embodiments for the present invention in such clear, concise and exact terms to enable any person of ordinary skill in the semiconductor processing art to use these techniques. These techniques are, however, susceptible to modifications and alternate implementations from those discussed above which are fully equivalent. Consequently, it is not the intention to limit the present invention to the particular embodiments disclosed. Rather, the intention is to cover all modifications and alternate implementations within the scope of the invention as set forth in the following claims. The following claims particularly point out and distinctly claim the subject matter of the present invention.